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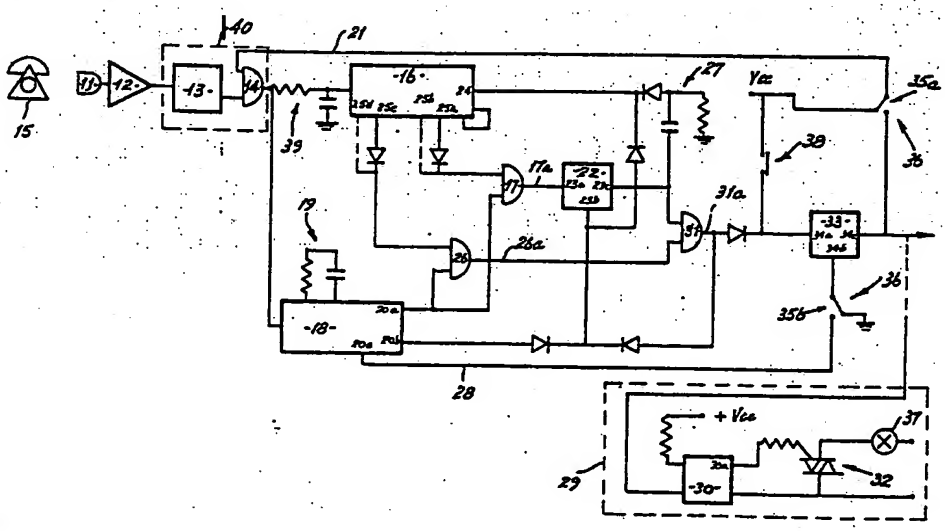

(57) Abstract

A control apparatus for controlling an electrical appliance (37) connected thereto in response to a series of coded input signals and particularly to the rings of a telephone (15). The apparatus includes an input stage which has an input signal pickup (11) and a pulse generator (40) for conditioning the input signals into an appropriate form. A counter (16) counts the conditioned input signals and outputs a count signal at the count outputs (25) indicative of the number counted. A timer (18) is reset by the input signals and produces various time signals at timing outputs (20) which correspond to different times from the last received input signal. A logic circuit decodes the coded input signals in response to count signals and time signals input thereto. An output circuit generates an output control signal and conveys the control signal to an appliance controller (29) which controls the appliance (37). Specific forms of pulse generator (40), logic circuit, and output circuit are defined herein.

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"Control Apparatus"

THIS INVENTION relates to a control apparatus which decodes an encoded input signal thereto and controls the operation of a device connected thereto in accordance with the encoded input signal corresponding to a predetermined code. Moreover, the invention relates to a control apparatus which decodes the rings of a telephone and electrically controls the operation of a device in accordance with coded groups of ring sequences.

The invention finds particular application with the control of operation of various electrical household appliances such as lighting systems, heating and cooling appliances, alarm systems audio and/or visual appliances and the like, wherein the operation of such devices may be enabled or disabled remotely using the rings of a telephone within a telephone network.

It has previously been known to provide remote control of various electrical household appliances in response to the ring of a telephone, but previous control apparatus employed in the interface between the appliance and the telephone receiver have all suffered from various disadvantages. Principal disadvantages of such prior art devices include cumbersome and expensive control apparatus, which can be susceptible to spontaneous or false triggering in response to input signals derived from sources not intended to activate control of an appliance. In situations where such prior art devices have utilized input ring signals from a telephone receiver, adequate provision has not been made to fully avoid possible false triggering of an appliance by stray telephone rings or calls, not intended for the control of the appliance.

An example of prior art in this field is described in United States Patent No. 3360777 issued to E.A. Kolm, which represents one of the early attempts at providing remote control of an appliance through utilization of the existing telephone network. This patent discloses a control apparatus employing a series of relays and timers to transfer the input signal through to the output of the device. Several problems are apparent with the adoption of such a device, principally the complicated and cumbersome nature of both the relays and timers employed therein. Furthermore, the device requires a different relay-timer combination to be used in response to each input signal. Thus it is impractical to implement a decoding system with this device, which requires the input of a predetermined number of groups of prescribed numbers of sequential input signals before an apparatus connected thereto is activated, an essential requirement of any remote control apparatus having an acceptable degree of immunity of false triggering.

Another example is described by United States Patent No. 3702904 issued to J.E. Bard. This device discards the expensive and cumbersome analogue circuit elements described within the Kolm reference, and employs a digital electronic device, in which a counter is controlled to count incoming telephone ring signals in accordance with the generation of a control signal, and an output means provides an indication of the number of rings counted. A disadvantage with this device results from the use of the particular control signal, described within the Bard reference, to determine operation of the counter, whereby the counter "being rendered operative to begin counting by a ring signal only in the absence of a first control signal". This feature, in addition to the very nature of the control signal, places a restriction on the further use of the counter and control signal in situations requi-

ring the decoding of groups of input ring sequences. The interaction between the counter and the control signal in this device favours the generation of an output signal indicative of the number of rings counted, in preference to the generation of an output signal in response to relatively complexly encoded ring signals. Thus in the latter application, the control means which generates the control signal does not lend itself to the efficient decoding of input ring signals.

Another device which is the subject of United States Patent No. 3783193 issued to M. Lee is also based on a remote control apparatus utilizing the telephone network. This device accepts two series of ringing signals, the first series activates a timer, which in turn enables a counter to count the second series of ringing signals, an appliance is activated in accordance with the second series of ringing signals equating a predetermined number. A disadvantage with this device resides in its inability to decode complexly encoded input ringing signals, since the first series of ringing signals is not required to conform to any particular code. Furthermore, the device does not provide for the decoding of a series of different groups of input ring sequences, and cannot be efficiently adapted to accommodate such.

Another example is the subject of United States Patent No. 4304967 issued to I. Gretczko, which is directed towards a device having a counter to count input countable signals, and a timer to control the counting of said input signals, whereby after the counter reaches a predetermined number of counted signals, an appliance connected thereto may be activated. A disadvantage with this device resides in its lack of decoding to avoid false triggering, whereby an appliance is activated immediately upon the receipt of a predetermined number of input signals. In addition, no

provision is made for the timer to control the decoding of more complexly encoded input signals.

Other devices have been proposed which are essentially variations of the above references, and some or all display similar disadvantages to those previously mentioned.

It is an object of the present invention to provide a control apparatus of the type herein defined, which is more efficient and economic to implement than those devices described in the aforementioned references.

It is a further object of the invention to provide a control apparatus which can be simply modified or adapted to decode relatively complexly encoded input signals of the kind herein defined.

It is another object of the invention to provide a control apparatus which can be simply modified or adapted to improve the immunity thereof to false triggering.

It is another object of the invention to provide a control apparatus which can be simply modified or adapted to provide independent control of more than one device connected thereto.

In one form the invention resides in a control apparatus for effecting control of a device connected thereto in response to an encoded input signal normally composed of a series of substantially regularly spaced input signals comprising:-

(a) counting means to count the receipt of said input signals and generate a count signal signifying the magnitude of the number of said input signals counted;

(b) timing means to generate a first time signal after a first predetermined time interval has elapsed from receipt of an input signal; and

(c) output means to control operation of said device in response to the input thereto of a count signal corresponding to a predetermined magnitude, and said first time signal;

wherein said first time signal is only generated if a subsequent input signal is not received within the first time interval from the last received input signal.

According to a preferred feature of the invention, the timing means is reset to an initial state upon receipt of said input signal.

According to another preferred feature of the invention, the output means includes one or more logic means which sequentially decode one or more sets of generated count signals and first time signals in accordance with a prescribed code, and generate an output control signal in respect thereof to effect control of said device.

According to another preferred feature of the invention, the control apparatus includes a resetting means to reset said counting means at some arbitrary time after the generation of said first time signal, whereupon said resetting means applies a reset signal to said counting means.

According to another preferred feature of the invention, a logic means has a prescribed code corresponding to at least two said sets of signals and includes gating means corresponding to different sets of signals and a control means to control operation of said gating means whereby

said gating means sequentially decodes said sets of signals and, in combination with said control means effects the generation of an output control signal.

According to another preferred feature of the invention, the gating means comprises a series of gates each accepting inputs corresponding to said count signal of predetermined magnitude and said first time signal, whereby a gated signal is generated at the output of a gate in accordance with the said prescribed code, a first gate having a count signal corresponding in code to the first set of signals and successive gates having count signals corresponding in code to a successive set or sets of signals, the gated signal of a last gate effecting the generation of an output control signal.

According to another preferred feature of the invention a logic means has an initial operative state corresponding to the selected operation of said first gate, wherein said control means sequentially provides selected operation of successive gates in response to the output of a previously selected gate.

According to another preferred feature of the invention, the timing means generates a second time signal after a second predetermined time interval has elapsed from receipt of an input signal, said second predetermined time interval being relatively longer than said first time interval, and said second time signal being generated only if a subsequent input signal is not received within the said second time interval from the last received input signal, whereby said logic means accepts an input corresponding to said second time signal, whereupon the logic means is reset to said initial state upon generation of said second time signal.

According to another preferred feature of the invention, the arbitrary time does not extend beyond the time of generation of said second time signal.

According to another preferred feature of the invention the control apparatus includes an input means to receive said encoded input signal having a pulse generating means to generate a pulse in response to the input of a prescribed sequence of input signals, wherein said pulse is applied to the counting means and timing means to facilitate counting and timing operations of said input signals respectively.

In another form the invention resides in a pulse generating means for generating an output pulse in response to a prescribed sequence of input signals, said sequence corresponding to the receipt of one or more input signals within a fixed time period, comprising a delay means and a sampling means wherein said delay means outputs an activating signal to said sampling means after a time delay from the receipt of an input signal, and said sampling means generates said output pulse only in response to the presence of an input signal and said activating signal, said time delay approximating said fixed time period.

This invention will be better understood by reference to the following description of several embodiments. The description is made with reference to the accompanying drawings wherein:-

Fig. 1 is a circuit diagram of a remote control apparatus as described in the first embodiment;
Fig. 2 is a circuit diagram of a remote control apparatus as described in the second embodiment;
Fig. 3 is a block diagram of a remote control network in accordance with the third embodiment;

Fig. 4 is a block diagram of a remote control network in accordance with the fourth embodiment;
Fig. 5 is a circuit diagram of the input stage of a remote control apparatus as described in the first embodiment.

The embodiments of the invention are directed to a remote control apparatus which is operable in response to the rings of a telephone. The function of the apparatus is to electrically control the operation of one or more devices connected thereto in accordance with the demands of a user, the user communicating with the apparatus by means of the standard telephone network.

The operation of the apparatus is dependent upon the correct input of a prescribed number of groups of ring sequences, each group being of a predetermined number of ring sequences and successive groups being separated in time by a time period which falls within a prescribed range.

A ring sequence is defined to be a set of one or more rings, wherein the set forms the fundamental ring tone of a telephone receiver, as prescribed by the telephone network employed. The present invention is described with reference to the ring sequence adopted by the Australian telephone network, which comprises two successive rings in relatively rapid succession followed by a comparatively long pause. It should be appreciated, however, that the scope of the invention is not limited thereto, and has equal application to ring sequences adopted by other telephone networks, such as in the U.S.A. or the U.K.

Now describing the first embodiment of the invention, specifically shown in Fig. 1, a ring signal pickup 11 is connected to or located near a telephone 15. The ring

signal pickup may be a magnetic pickup connected directly to the receiver circuitry of the telephone or alternatively may be an acoustic microphone located near the telephone. The ring signal pickup 11 essentially produces a signal at the output thereof in response to the ringing sound of the telephone 15. The output of the ring signal pickup is connected to an amplifier and filter network 12 which in turn is connected to the input of a pulse generator logic circuit 40. The pulse generator logic circuit comprises a ring pulse generator 13 and an input logic gate 14. The ring pulse generator 13 is designed to generate a single ring pulse at the output thereof for each ring sequence produced by the telephone 15. The output of the pulse generator 13 is connected to one input of the logic gate 14, which is configured as an AND gate. A feedback line 21 is connected to a second input of the input logic gate 14 and is derived from the output 34c of an output flip-flop 33 via a switch 36, to be described later, whereby the logic gate 14 can either block or pass ring pulses therethrough in accordance with the state of the feedback line 21.

The output of the gate 14 is connected directly to the reset pin of a timer 18, and via an RC delay network 39 to the clocking input pin of a counter 16. The timer 18, is preferably a large bit binary counter (eg. 14 bit) with the clocking frequency thereof set by means of an RC circuit 19 to facilitate the production of a relatively long time delay (eg. 5 hours). The timer is set to count continually whilst the control apparatus is in operation, by means of an oscillator. Three timing outputs 20a, 20b, 20c are taken from the timer 18, respective timing outputs 20 equating successive prescribed time periods from the last reset pulse received by the timer. The first timing output 20a is chosen to be asserted upon the expiration of a first time period T1 (approximately 10 seconds) from

the time of the last received resetting pulse. The second timing output 20b is chosen to be asserted upon the expiration of a second time period T2 (approximately 1 minute), from the time of the last received resetting pulse and is greater than time period T1. Lastly, the third timing output 20c is chosen to be asserted upon the expiration of a third time period T3 (approximately 5 hours), from the time of the last received resetting pulse, and is substantially greater than both the first and second time periods T1 and T2 respectively. These time periods are selected such that: T1 is longer than the normal time interval between successive sets of ring sequences but less than some nominal minimum time that it would take a caller to terminate a telephone call to the telephone 15 and re-dial the number of the telephone 15; T2 is longer than the latter minimum time but less than some nominal maximum time that would enable a caller to at least re-dial the telephone once; and T3 is some maximum time greater than both T1 and T2, whereupon the state of the output of the control apparatus may be reset to its original condition automatically after the initial selection of the control function. The latter is defined as the timing mode of the control apparatus and will be described in further detail hereinafter.

The counter 16, is preferably a sequential decade counter which successively asserts sequential counter outputs 25 in accordance with received ring pulses. The counter is reset at pin 24 which has lines connected thereto from the second timing output 20b, the output 31a of an output logic gate 31, to be described later, and the output of an intermediate flip-flop 22, also to be described later. A first preselected counter output 25a, is connected to an input pin of a first intermediate logic gate 17 and a second preselected counter output 25c, is connected to an input pin of a second intermediate logic gate 26. The

first timing output 20a is connected to the other input pin of both intermediate gates 17, 26 which are both configured as AND gates. The first preselected counter output 25a is selected to correspond, when asserted, to a first number of received ring pulses counted by the counter 16, and the second preselected counter output 25c similarly corresponds to a second number of received ring pulses. Thus, the assertion of either output line 17a, 26a from intermediate logic gates 17, 26 respectively, is dependent upon the simultaneous assertion of respective inputs derived from counter outputs 25a, 25c, with the first timing output 20a.

The output 17a of the first intermediate logic gate 17 is connected to the set input 23a of the intermediate flip-flop 22, which is configured as a J-K flip-flop. The second timing output 20b and the output 31a of the output logic gate 31 are both connected to the reset pin 23b of the intermediate flip-flop 22. Thus the flip-flop 22 is set, i.e. the output 23c thereof asserted, when the first intermediate gate output 17a is asserted, and is reset, i.e. the output 23c thereof negated, when either the second timing output 20b or the output logic gate output 31a is asserted.

The output 23c of the intermediate flip-flop 22 is connected as one input to the output logic gate 31, and in addition, is fed back via an RC delay network 27 to the reset pin 24 of the counter 16. Accordingly, the counter 16 will be reset shortly after the initial assertion of flip-flop output 23c. The output logic gate 31, being configured as an AND gate, obtains its other input from the second intermediate logic gate output 26a. Accordingly, upon the simultaneous assertion of flip-flop output 23c and logic gate output 26a, the output logic gate output 31a will be asserted. The gate output 31a is fed back

to both the intermediate flip-flop reset pin 23b and the counter reset pin 24, and is connected to the toggle input 34a of an output flip-flop 33, configured in a toggling mode. The reset input 34b of the output flip-flop 33 is obtained from the third timing output 20c of the timer 18 along reset line 28. As referred to previously, the output flip-flop output 34c is connected via feedback line 21 to an input pin of the input logic gate 14. Integral switches 35a, 35b of a double pole double throw (DPDT) switch arrangement 36 are respectively connected along the feedback line 21 and reset line 28 to provide selective operation of the control apparatus in either a timing mode or toggling mode.

In the timing mode, switches 35a, 35b are positioned to connect lines 21, 28 directly to the output flip-flop's output 34c and reset 34b pins respectively. In the toggling mode, switches 35a, 35b are switches to the alternate position wherein line 21 is connected directly to a voltage supply rail Vcc and line 28 is open circuited (reset input 34b being connected to ground).

Provision is made for a push button switch 38 connected between the voltage supply rail Vcc and the output flip-flop toggle input 34a, to facilitate manual timing of the output flip-flop 33.

The output flip-flop output 34c forms the output control line of the control apparatus and may be utilized in a number of ways. In the present embodiment, the flip-flop output 34c is connected to a device controller 29, which comprises an opto coupler 30 and a triac 32. The flip-flop output 34c is connected to the input of the opto coupler 30. The output 30a of the opto coupler 30, being isolated and remotely situated from the input side thereof, is connected to the gate lead of the triac 32. The

triac 32 is connected in series with the AC power supply lines of a device 37 which is to be controlled by the control apparatus.

Now describing the ring pulse generator 13 of the control apparatus in more detail, as shown in Fig. 5, the pickup is represented at 101 and is connected at B to an amplifier and filtering network 102. A filtering and rectifying stage 103 comprising capacitors and diodes is connected to the output of the network 102, and is included to convert the AC output signal from the stage 103 to DC. The converted DC signal is subsequently applied to the clock input of a J-K flip-flop 104 set in a non-retriggerable monostable mode, i.e. the J pin connected to ground, and the K pin connected to the supply rail. The output of the J-K flip-flop 104 is configured such that a voltage divider comprising resistors 105a, 105b is connected across the Q and reset pins, Q and R respectively and an output capacitor 106 is connected in series with both the voltage divider and reset pin R. An output logic gate 107, configured as an AND gate, accepts one input from the output of the voltage divider 105 and another from the DC signal which is applied to the flip-flop 104. The output A of the output logic gate 107 forms the output of the ring pulse generator 13 and is applied to the input logic gate 14 as previously described.

Now describing the operation of the ring pulse generator, DC signals corresponding to ring signals of the telephone 15, are applied to the clocking input of the J-K flip-flop 104. These signals are generated in pairs, integral signals having a period of approximately 0.75 seconds, and pairs of signals having a period of approximately 3 seconds.

The first signal of a said pair triggers the monostable, and a logic high is output at Q having a duration determined by the time constant of the output capacitor 106 and resistor. That is, the capacitor 106 slowly charges up in response to the logic high at Q until the voltage produced at the reset pin R is sufficient to reset the J-K flip-flop 104. The time constant of the capacitor is set such that the duration of the logic high at Q is slightly longer than the period of said integral signals applied to the flip-flop 104. Accordingly, the output of the voltage divider 105 approaches the threshold voltage for a logic high at the input of the output logic gate 107, just prior to the resetting of Q, and during the presence of the second signal of the said input pair of signals. Therefore the voltage divider output will strobe the value of the input signal to the flip-flop 104, through to the output A of the output logic gate. Thus a ring pulse is generated at A if and only if the monostable is triggered at a first time, and within approximately 0.75 seconds from the first time, the input to the monostable is active.

A significant advantage of this type of ring pulse generator, is that the control apparatus can be used without modification with both Australian and United States telephone networks. In addition, as the ring pulse generator effectively samples the signal applied thereto for a relatively short sampling period in response to an initial triggering signal, at a predetermined time after the initial triggering signal, erroneous generation of ring pulses in response to noise or stray voltage spikes, is largely avoided.

In an alternative arrangement, the output of the J-K flip-flop 104 is configured such that an RC delay network is connected across the Q and reset pins of the flip-flop,

and the $\bar{Q}$ output of the flip-flop is connected via a differentiator network to the input of the output logic gate 107. The other input of the output logic gate being derived from the input to the flip-flop 104, as in the previous arrangement. The operation of this arrangement is substantially similar to the previous arrangement, wherein the incoming signal triggers the monostable, and a sample of the input signal is taken approximately 0.75 seconds later, the state of the input at this time being strobed through the output logic gate. However, in the present arrangement the $\bar{Q}$ output is utilized to generate a strobing pulse from the differentiator to sample the input signal. In more detail, the incoming first signal of a signal pair, triggers the monostable such that the Q output is high and the $\bar{Q}$ output low. The capacitor in the RC delay network charges and eventually asserts the reset pin R of the flip-flop 104 at approximately 0.75 seconds from the time of the triggering signal. The resetting of the flip-flop causes the $\bar{Q}$ output to return to high, thereby causing the differentiator to output a short pulse which in turn strobes the input signal at that time through the output logic gate 107. If the input pair of signals have a period of approximately 0.75 seconds, the second signal of the pair will be detected and cause the output logic gate 107 to output a ring pulse.

Now describing the operation of the first embodiment of the invention, ringing signals from telephone 15 are picked up by the ring signal pickup 11, and are amplified and filtered by the amplifier and filter network 12 to remove extraneous noise. A signal corresponding to the rings is input to the pulse generator logic ciruit 40, wherein the pulse generator 13 produces one ring pulse for every set of 2 rings (assuming the normal Australian telephone ringing convention). This ring pulse is input to the input logic gate 14 which either blocks or passes

the ring pulses depending on the state of the feedback line 21.

As each ring pulse passes through the gate 14 it resets the timer 18 which subsequently produces a low state on each of its binary timing outputs 20. In addition the said ring pulse is input to the decade counter 16 via the RC delay network 39, as a clocking pulse. Thus as each ring pulse occurs the timer 18 is repeatedly reset and the counter 16 counts the number of successive ring pulses. When a predetermined number of ring pulses have been input to the counter 16, the first count output 25a thereof is asserted and remains active for the time during which the number of received ring pulses corresponds to the said predetermined number. In addition, upon the timer 18 reaching the first timing period T1 (say 10 seconds) from the last resetting ring pulse received the first timing output 20a will be asserted, subject to there being no subsequent ring pulse generated during this period. Thus upon the concurrent activation of the first count output 25a and the first timing output 20a, the output 17a of the first intermediate logic gate 17 will be asserted thereby causing an output pulse to set the intermediate flip-flop 22, indicating that a first set of rings has been correctly received. Consequently, the setting of intermediate flip-flop 22 causes the counter 16 to be reset by applying the flip-flop output 23c to the reset pin 24 of the counter 16, thereby enabling the counter 16 to be used again for further counting of ring pulses. This process of setting the flip-flop 22 will only occur if the telephone ringing stops at the correct number of rings for at least a first time period T1 (10 seconds) but less than the second time period T2 (say 1 minute).

If the telephone 15 rings for more or less than the prescribed number of rings, counter 16 will eventually cease

counting after the last counter output has been asserted, and if no further rings are received within a second period T2, then the second timing output 20b from timer 18 will be asserted and will reset the intermediate flip-flop 22 via reset input 23b, and reset the counter 16 via reset pin 24, thereby initializing the apparatus for receipt of a new set of rings. Thus the apparatus is substantially immune to responding to incorrect sets of rings.

After the first group of rings has correctly actuated the intermediate flip-flop 22, the caller can re-dial the number of the telephone 15 and generate a second group of ringing signals which in turn are picked up by the ring signal pickup 11, passed through the amplifer and filter network 12 to the pulse generator 13. Ring pulses produced by the pulse generator can then be applied to the counter 16 and the timer 18 via the input logic gate 14. As described previously, the ring pulses continually reset the timer 18 and increment the counter 16. When the second group of rings reaches the predetermined number (which may be a different number of rings than the first group), the second counter output 25c of counter 16, is asserted. Accordingly, if and only if the rings cease at the correct number which corresponds to the second counter output 25c, for more than a period T1 (ten seconds), will the output 26a of the second intermediate logic gate 26 be asserted. If this output 26a is asserted when the output 23c of intermediate flip-flop 22 is set, the output 31a of the output logic gate 31 will consequently be asserted. Upon the assertion of the output logic gate output 31a, the output 34c of the output flip-flop 33 changes state, and, in addition, the counter 16 and intermediate flip-flop 22 are both reset, thereby initializing the control apparatus for receipt of a new set of rings.

The output 34c accordingly controls the operation of the external device 37 by triggering or switching off the triac 32. Thus by a caller dialling the number of the telephone 15 and providing the correct combination of ring sequences to the control apparatus and generating the second ring sequences within, time period T2 of the first ring sequence, the control apparatus can either switch a device on or off.

Should the second series of rings be within a second period T2 (1 minute) but be of an incorrect number, then the second intermediate logic gate output 26a will not be asserted and subsequently output logic gate output 31a will not be asserted. Therefore the timer 18 will increment until second timing output 20b is asserted (after period T2), which will reset counter 16 and intermediate flip-flop 22, thereby initializing the apparatus for receipt of a new set of rings.

In order to cater for errors inherent within the telephone network due to possible variations in the number of received rings as compared to the number of ring back tones heard by the caller, counter outputs 25b, 25d adjacent to respective first and second counter outputs 25a, 25c, may be connected via diodes to the respective inputs of intermediate logic gates 17, 26 in addition to counter outputs 25a, 25c, whereby the first and second counter outputs form an OR gate function with adjacent outputs. Thus provision is made for the acceptance of not only the prescribed number of rings within a group of rings, but perhaps a number corresponding to one more, or one less than the prescribed number. It should be noted that this type of allowance is facilitated by the adoption of a sequential decade counter as the counter 16.

As mentioned previously, the control apparatus can be selectively switched for operation in either a timing mode or toggling mode. With switch 36 set in the timing mode, the input logic gate 14 is controlled by the state of the output flip-flop output 34c. When the output flip-flop 33 is in its initial state, eg. the device controller 29 being arranged to keep the device 37 in an off state, feedback line 21 is asserted thereby allowing the input logic gate 14 to pass ring pulses to the timer 18 and counter 16. Upon receipt of correct combination of ring pulses, the output flip-flop 33 will be toggled such that the output 34c thereof will change state. This change of state will enable the device controller to switch on the device 37 and additionally will be fed back along feedback line 21 to the input gate 14, and in so doing will disable the gate. Accordingly the input logic gate 14 will block any further ring pulses input thereto, thereby enabling the timer 18 to ultimately time through its third time period T3, whereupon the third timing output 20c thereof will be asserted. As the third timing output 20c will be connected to the reset pin 34b of the output flip-flop 33, the output flip-flop output 34c will be reset to its previous state, thus switching the device 37 off automatically and enabling the input logic gate 14 to pass ring pulses once again. With the control apparatus in the timing mode, it is possible for a user of the apparatus to remotely switch on a device 37 connected thereto by calling the telephone 15 with the correct combination of rings, whereinafter the device will remain on a prescribed period determined by the length of third time period T3, after the expiration of which the device will be automatically switched off. During the period the device remains on, the control apparatus automatically disables itself from accepting any further ring pulses.

With the switch 36 set in the toggling mode, the input logic gate 14 is always enabled along feedback line 24, therefore all ring pulses that are applied thereto will be passed onto the timer 18 and counter 16. It can also be seen that in this mode, the third timing output 20c has no effect upon the state of the output flip-flop 33. Thus the output flip-flop 33 continually performs a toggling function, changing its state upon each set of correctly coded groups of ring signals received by the telephone 15.

The second embodiment of the invention is substantially similar to the first embodiment wherein the input stage of the control apparatus which receive ringing signals and generates ring pulses in respect thereof is identical. With reference to Fig. 2, generated ring pulses are input from A to an input logic gate 51, A corresponding to the output of a pulse generator as in the first embodiment. The input logic gate 51 is connected the same as in the previous embodiment, wherein its other input 52 is derived from the output 71c of an output flip-flop 70 via a switch 72. Similarly, the input gate 51 either blocks or passes incoming ring pulses in accordance with the state of its other input 52. The output of the input gate 51, likewise, is connected to the reset pin 53 of a timer 54 and via an RC delay network 57 to the clocking input 58 of a counter 59.

As in the previous embodiment, the timer 54 is a large bit decade counter which operates continuously in a counting mode by means of an oscillator, the frequency of which is determined by the RC circuit 56. Again, three timing outputs 55a, 55b, 55c are obtained from the timer 54, which respectively correspond to the three time periods T1, T2, T3 described in the first embodiment.

The counter 59, again, is a sequential decade counter having sequential counter outputs 60. Certain counter outputs, corresponding to prescribed numbers of input ring pulses counted, are connected to intermediate logic gates 63. As shown in Fig. 2, counter output 60a connects to one input of input logic gate 63a, each intermediate logic gate being a three input AND gate, counter output 60b connects to an input of gate 63b, and so on. The second inputs to intermediate logic gates 63 are all obtained from the first timing output 55a of the timer 54. Additionally the timing output 55a is connected by way of another RC delay network 65 to the reset pin 62 of the counter 59. The third inputs to the intermediate logic gates 63 are derived from an intermediate counter 67, which will be presently described.

The intermediate counter 67 is identical to the counter 59, being a sequential decade counter. However, the intermediate counter accepts clocking inputs at its clock input pin 68, from any of the intermediate logic gate outputs 64. Additionally, successive counter outputs 69a, 69b are respectively connected as the third inputs to successive intermediate logic gates 63a, 63b, and the last selected counter output 63c, successive to counter output 69b, is connected directly to the toggle input 71a of the output flip-flop 70.

The counter 59 has lines to its reset pin 62 from either the second timing output 55b of the timer 54, and intermediate logic gate outputs 64, or alternatively from the first timing output 55a (previously mentioned), thus the counter is reset to zero upon, or some delay time after, the assertion of any of these lines.

The second timing output 55b, not only provides a resetting pulse to the counter 59, but also provides a resetting

pulse to the intermediate counter 67 by way of connection to resetting input 66.

The output flip-flop 70 is similarly configured to that in the first embodiment, wherein it has its reset input 71b connected to the third timing output 55c of the timer 54, and its output 71c drives a device controller connected at B, which in turn controls the operation of an external device by means of a triac or relay (not shown). In addition a similarly configured DPDT switch 72 enables a choice in operating the control apparatus in the previously described timing mode or toggling mode. Similarly, a push button switch 73 is included between the supply Vcc and the output flip-flop input 71a to facilitate manual operation of the output circuitry of the apparatus.

Now describing the operation of the second embodiment, ring pulses are received by the input logic gate 51 at A, in accordance with the first embodiment, and are either blocked or passed, depending upon the state of input 52. Assuming that input 52 is asserted (this may be due to the apparatus being set in the toggling mode, or the initialized stage of the timing mode), ring pulses will be input to the reset input of the timer 54, and after a short delay, counted sequentially by the counter 59.

As with the previous embodiment, the timer 54 will be reset upon the receipt of every ring pulse generated. Thus when a series of ring pulses are received, the timer 54 will be continually reset until the ring pulses have stopped for a time period T1, T2 or T3 before respective timing outputs 55a, 55b, or 55c are asserted.

The counter 59 asserts one counter output 60 at a time in sequence such that the assertion of a counter output corresponds to the ordinal number of ring pulses input to

the counter 59 at that time. In both embodiments described thus far, decade counters have been used at the principal ring pulse counting means, therefore it is only possible to count to a maximum of 10 input ring pulses, however, it is possible to cascade additional decade counters to the principal counters with appropriate decoding circuitry, thereby enabling any number of ring pulses to be counted.

Counting a first series of ring pulses, first counter output 60a will be asserted when a corresponding number of ring pulses have been input to the counter 59. If no further ring pulses are received within first time period T1 (say 10 seconds) from the time of the last received ring pulse, then first timing output 55a is asserted. The intermediate counter 67 is initialized such that its first counter output 69a, corresponding to zero clocking inputs received at clock input 68, is asserted. Being a sequential decade counter, all other counter outputs 69 will be negated. Accordingly, during receipt of the first series of ring pulses, the first intermediate logic gate 63a is selected by the intermediate counter output 69a, and the gate output 64a will be asserted upon receipt of a strob ing pulse from the first timing output 55a, if and only if the last received ring pulse has asserted first counter output 60a. Thus the first intermediate gate output 64a will only be asserted when each of the three inputs to the gate 63a are simultaneously active.

The delay network 65 works to delay receipt of the asserted first timing output 55a by the counter reset input 62, until after the first intermediate logic gate 63a has been strobed by the first timing output. Subsequently, the counter 59 will be reset to zero by the action of the delayed first timing output 55a or the intermediate gate output 64a. Additionally, the assertion of the first

intermediate gate output 64a clocks the intermediate counter 67 by way of clock input 68, and thus the successive second counter output 69b will be asserted, thereby priming the second intermediate logic gate 63b.

Now a second series of ring pulses are required to be input to the timer 54 and counter 59 before the second time period T2 expires, otherwise the second timing output 55b will be asserted, thus resetting the intermediate counter 67 back to zero, and thereby negating second counter output 69b and priming the first intermediate gate 63a once again. If a second series of ring pulses are received within second time period T2, the timer will be reset once again and the second series of ring pulses counted by the counter 59. If the second series of input ring pulses stops at a number corresponding to the assertion of second counter output 60b, the second intermediate gate 63b will be strobed after a first time period T1 by the assertion of the first timing output 55a. Accordingly the second intermediate gate output 64b will be asserted, thus clocking the intermediate counter 67 to assert its next counter output 69c. In addition, the assertion of the first timing output 55a or the second intermediate gate output 64b causes the counter 59 to be reset back to zero.

The present embodiment is arranged such that upon assertion of the third counter output 69c the output flip-flop 70 will be toggled thereby issuing a control signal at the flip-flop output 71c which may be utilized in a manner described in the previous embodiment.

It should be evident from this and the previous embodiment, that should an incorrect number of ring pulses be counted by the counter at any stage, the appropriate intermediate logic gate will not have its output asserted and thus the intermediate counter will not be clocked.

Accordingly, the assertion of the second timing output 55b will eventually reset the entire apparatus after second time period T2 has expired.

It should be appreciated that in both the first and second embodiments, the number of groups of ring sequences required to be input by a user of the control apparatus is two. However, this number may be easily extended in both circuits by increasing the complexity of the intermediate circuit stage in each instance. In the first embodiment, this can be done by simply adding further intermediate logic gates and intermediate flip-flops such that the actuating signal may be clocked successively therethrough in accordance with groups of ring sequences. The bulkiness of such an arrangement is overcome by the second embodiment, wherein it is only necessary to introduce further intermediate logic gates 63 and connecting successive intermediate counter outputs 69 thereto, such that the last counter output is connected to the output flip-flop input 71a. Additional intermediate counters may be cascaded to the primary intermediate counter to facilitate counting of groups of input ring sequences greater than ten. Appropriate decoding circuitry will be required for the implementation of this arrangement, however.

The third embodiment of the invention is directed towards a remote control network, wherein it is possible to control the operation of a number of external devices, each having a unique code for remote control thereof, and each being connected to the output of a control apparatus of the kind described in either of the previous embodiments.

With specific reference to Fig. 3, the input stage of a control apparatus as described in the first and second embodiments is represented at 81. The input stage 81 comprises the previously described ring signal pick up and

conditioning circuitry, the ring pulse generator and logic circuitry, and the timer and counter circuits. The intermediate stage of the control apparatus is represented at 82, and comprises intermediate logic circuitry and intermediate flip-flops or counters in accordance with the relevant embodiment hereinbefore described. A series of intermediate stages 82 are provided, each connected to a corresponding output flip-flop 83 and device controller 84.

Each intermediate stage 82 is designed to uniquely decode groups of input ring sequences derived from the input stage 81, such that differently coded input ring sequences may operate or toggle different devices connected to corresponding intermediate stages 82 via device controllers 84 and output flip-flops 83.

Describing the operation of this embodiment in further detail, the input stage 81 receives ring signals from a telephone (not shown) and accordingly activates timer and counter circuits as described in the previous embodiments. A series of differently encoded intermediate stages 82 are connected to the input stage 81 such that upon receipt of a prescribed input code of ring sequences, one or more correspondingly encoded intermediate stages 82 will decode the input code and thus toggle the output flip-flop 83 connected thereto. The output flip-flip 83 will in turn apply its altered output signal to its corresponding device controller 84 which will subsequently alter the operation of the corresponding device connected thereto as described in the previous embodiment.

As in each of the previous embodiments, when the toggling mode of operation is selected, after the expiration of the second time period T2, the entire network will be reset, thus enabling a caller to initiate a further series of

coded ring sequences, which may change the operation of the previously selected device back to its original state, or similarly alter the operation of another device by selecting another prescribed code. Similarly, various devices may be controlled with the control apparatus operating in the timing mode, wherein coded input signals may be blocked by the corresponding control apparatus of a previously selected device until the third timing period T3 has expired.

The fourth embodiment is directed towards an improved remote control network, as described in the third embodiment, which provides control of an increased number of device controllers and devices connected thereto with respect to the number of intermediate stages provided. Reference is made to Fig. 4, wherein a remote control network, as described in the previous embodiment, has an input stage 91 connected to three different intermediate stages 92a, 92b, 92c having corresponding output flip-flop's 93a, 93b, 93c.

The output of each of the output flip-flops 93 is connected to the input data select pins 96a of a decoder/demultiplexer 95. In this embodiment the decoder/demultiplexer is a 3-line-to-8-line type, wherein the three data select pins 96a are decoded to select one of eight output lines 96c, each of which are connected to an associated device controller 94 and external device (not shown).

A fourth timing output 97 is taken from the timer within the input stage 91, which is asserted upon the expiration of a fourth timing period T4, timing period T4 being chosen arbitrarily to correspond to a period of approximately 5 minutes from the last received input ring pulse. This timing output 97 is connected to enable pin 96b of the decoder/demultiplexer 95, such that the decoder/demul-

tiplexer is enabled to decode the input data select pins 96a only when the fourth timing output 97 has been asserted.

Thus, in operation, a caller is required to set the output of each output flip-flop 93 by inputting the correct combination of groups of ring sequences for that particular flip-flop, such that the outputs of the output flip-flops 93 form a prescribed code for decoding by the decoder/demultiplexer 95 so that the operation of a selected device 94 may be altered. After the last flip-flop has been set to the desired state, the timer will eventually assert the fourth timing output 97 after the expiration of timing period T4, thereby enabling the decoder/demultiplexer 95, and thus the selected device controller 94 will be activated to alter the operation of the device connected thereto.

It should be noted that in practice, it is not desirable to have a device controller and associated device connected to an output line corresponding to an input data select of the output flip-flops in their initialized state, eg. 000, as such a device would be selected from any anomolous telephone call, whereinbefore no output flip-flop had been set, because the timer would still assert its fourth timing output and thus activate the decoder/demultiplexer. Thus with N input data select lines connected to a decoder/demultiplexer, it would be possible to control 2^N-1 device controllers and associated devices.

According to a fifth embodiment of the invention, the remote control apparatus may incorporate means for providing a confirmation signal in response to the acceptance of a correct set of rings. Such means may comprise a solenoid which will lift the telephone handset on the called

telephone for a predetermined time, say 5 minutes, thereby enabling the called telephone to produce an engaged tone signal to further callers during the time of actuation of the solenoid.

Now discussing the advantages of the invention, firstly false or erroneous triggering of the control apparatus to the extent of actuating or deactuating a device connected thereto is extremely difficult due to the requirement that a number of groups of differently numbered ring sequences must be input within a prescribed time to control the operation of such a device connected thereto. Accordingly, it is essential to know the correct combination of ring sequences if the device is to be remotely controlled.

The present invention is easily adapted to cater for any number of input groups and input ring sequences within a group to effect control of a device thus providing greater security. In addition, it is possible to adapt the apparatus to accept two or more different adjacent numbers of ring sequences within a group to cater for possible errors in the number of ring tones heard by the caller in relation to the actual number of ring sequences produced by the telephone receiver at the location of the control apparatus.

The apparatus can be easily adapted to operate a network of external devices connected thereto, each requiring a unique combination of groups of ring signals for control thereof. Thus control of the device can be independently actuated (or deactivated) by ringing the unique code of groups of ring sequences corresponding to that particular device only.

It is possible to employ various decoding techniques at the output of the apparatus to facilitate selection or

control of a large number of external devices connected to a single control apparatus.

An important feature of the present invention is the adoption of a single integrated circuit counter to perform all the timing functions of a timer with a high degree of accuracy, including a variable long delay timer to automatically turn-off a device.

Another important feature is the adoption of a single integrated circuit counter which combines with the intermediate stage of the circuit to decode multiple ring sequences of up to ten rings with provision for easy accommodation of larger numbers of ring sequences.

Thus it is possible to operate a complex control network with single timer and counter circuits.

Provision is made for selective operation of the control apparatus in either a timing mode or toggling mode as hereinbefore described.

In addition, a facility is provided to change the state of the output of the controller manually by means of a push-button switch without the need to apply ringing signals to the unit.

It should be appreciated that the scope of the present invention need not be limited to the scope of the particular embodiments described herein. Particularly, the intermediate flip-flop described herein, need not be limited to a J-K flip-flop but may comprise any convenient storage or memory element capable of recognising the assertion of an input thereto, and maintaining an output thereof in an active state upon said recognition for a predetermined time period. For example the intermediate storage element

may be a capacitor having a sufficiently long time constant to accept a charge input thereto and retain the charge for at least a time corresponding to the second time period T2 described within the embodiments herein.

Likewise, the output flip-flop may comprise any suitable storage or latching element to facilitate production of an output signal. Indeed, in an extremely simple arrangement of the invention, the output signal may be obtained directly from the second intermediate flip-flop or intermediate counter, in accordance with the appropriate embodiment described herein.

It should also be appreciated that the invention is not limited to operating in a timing or toggling mode as described herein, but can be arranged, without departing from the scope of the invention to include an embodiment wherein one prescribed code of ring sequences always activates a device connected to the apparatus, and a different prescribed code of ring sequences always de-activates the device. In this way, it is possible for a caller to repeatedly generate a prescribed code any number of times to ensure that a device is either activated or de-activated.

Again, without departing from the scope of the invention, it is possible to have the control apparatus situated remotely from the telephone receiver whereby ring signals may be conveyed to the apparatus by any appropriate transmission medium, for example by means of the AC mains wiring within a building, by RF or microwave links, or opto-coupling means.

In addition, it should be appreciated that the present invention is not limited to application wherein activation of the apparatus is provided solely by a telephone net-

work. For example, the control apparatus may be employed in any type of communication system wherein actuation of a device can only be effected upon the input of prescribed encoded signals. Thus the clocking speeds of the timer can be easily adjusted to facilitate operation of the device in a higher frequency environment, for pulse train decoding and sequential signalling applications.

Further, it should be appreciated that the scope of the invention is not limited to the particular types of counters and timers described herein but has application to other forms available, wherein, for example, different independent timers may be controlled to generate the various time signals hereindescribed.

THE CLAIMS defining the invention are as follows:-

1. A control apparatus for effecting control of a device connected thereto in response to an encoded input signal normally composed of a series of substantially regularly spaced input signals comprising:-

(a) counting means to count the receipt of said input signals and generate a count signal signifying the magnitude of the number of said input signals counted;

(b) timing means to generate a first time signal after a first predetermined time interval has elapsed from receipt of an input signal; and

(c) output means to control operation of said device in response to the input thereto of a count signal corresponding to a predetermined magnitude, and said first time signal;

wherein said first time signal is only generated if a subsequent input signal is not received within the first time interval from the last received input signal.

2. A control apparatus as claimed at claim 1, wherein said timing means is reset to an initial state upon receipt of said input signal.

3. A control apparatus as claimed at claims 1 or 2, wherein said output means includes one or more logic means which sequentially decode one or more sets of generated count signals and first time signals in accordance with a prescribed code, and generate an output control signal in respect thereof to effect control of said device.

4. A control apparatus as claimed at any of the preceding claims wherein said control apparatus includes a resetting means to reset said counting means at some arbitrary time after the generation of said first time signal, whereupon said resetting means applies a reset signal to said counting means.

5. A control apparatus as claimed at claims 3, 4 and any of the preceding claims wherein a logic means has a prescribed code corresponding to at least two said sets of signals and includes gating means corresponding to different sets of signals and a control means to control operation of said gating means, whereby said gating means sequentially decodes said sets of signals and, in combination with said control means, effects the generation of an output control signal.

6. A control apparatus as claimed at claim 5, wherein said gating means comprises a series of gates each accepting inputs corresponding to said count signal of predetermined magnitude and said first time signal, whereby a gated signal is generated at the output of a gate in accordance with the said prescribed code, a first gate having a count signal corresponding in code to the first set of signals and successive gates having count signals corresponding in code to a successive set or sets of signals, the gated signal of a last gate effecting the generation of an output control signal.

7. A control apparatus as claimed at claim 6, wherein said logic means has an initial operative state corresponding to the selected operation of said first gate, wherein said control means sequentially provides selected operation of successive gates in response to the output of a previously selected gate.

8. A control apparatus as claimed at claim 7 wherein said timing means generates a second time signal after a second predetermined time interval has elapsed from receipt of an input signal, said second predetermined time interval being relatively longer than said first time interval, and said second time signal being generated only if a subsequent input signal is not received within the said second time interval from the last received input signal, whereby said logic means accepts an input corresponding to said second time signal, whereupon the logic means is reset to said initial state upon generation of said second time signal.

9. A control apparatus as claimed at claims 4 and 8, wherein said arbitrary time does not extend beyond the time of generation of said second time signal.

10. A control apparatus as claimed at claim 4 and any of the preceding claims wherein said reset signal is generated in response to the generation of said first time signal.

11. A control apparatus as claimed in claim 9, wherein said reset signal is generated in response to the generation of said second time signal.

12. A control apparatus as claimed at claim 6 and any of the preceding claims, wherein said control means includes an intermediate counting means, the output of a gate providing a clocking input thereto, whereupon successive gates are sequentially selected by the output of said intermediate means upon a selected gate generating a gated signal.

13. A control apparatus as claimed at claim 12 wherein the said gated signal of the last gate clocks said inter-

34. A control apparatus as claimed at claim 29 and any of the preceding claims wherein said pulse generating means comprises a delay means and a sampling means, whereby said delay means outputs an activating signal to said sampling means after a time delay from the receipt of an input signal, and said sampling means generates said pulse only in response to the presence of an input signal and said activating signal, said time delay approximating said fixed time period.

35. A control apparatus as claimed at claim 34, wherein said delay means comprises a monostable multivibrator, triggerable in response to a received input signal, and a charging means including a capacitor, said charging means being actuated by the triggering of said monostable, whereby said monostable charges said capacitor to at least a threshold voltage, said threshold voltage causing the monostable to reset, and the charging means generating said activating signal at a time near or in conjunction with the capacitor attaining said threshold voltage.

36. A control apparatus as claimed at claim 35 wherein said charging means includes an integrating circuit which integrates the non-inverted output of said monostable to effect generation of said activating signal.

37. A control apparatus as claimed at claim 36, wherein said charging means includes a voltage divider in series with said capacitor whereby said activating signal is generated at the output of the voltage divider.

38. A control apparatus as claimed at claim 35, wherein said charging includes a differentiating circuit which differentiates the inverted output of said monostable to effect generation of said activating signal.

39. A control apparatus as claimed at any of claims 34 to 38, wherein said sampling means comprises a logic gate having one input corresponding to said input signal and another input corresponding to said activating signal, whereby said pulse is generated in response to the concurrent presence of an input signal and activating signal.

40. A control apparatus as claimed at claim 4 and any other claims dependent thereon, wherein said resetting means is said timing means.

41. A control apparatus as claimed at any of the preceding claims wherein said timing means is a single integrated counter.

42. A control apparatus as claimed at claim 41, wherein said counter is a binary counter.

43. A control apparatus as claimed at any of the preceding claims wherein said counting means includes decoding means to provide an output count signal in response to said generated count signal corresponding to a number of different predetermined magnitudes.

44. A control apparatus as claimed at any of the preceding claims wherein said counting means is a single integrated counter.

45. A control apparatus as claimed at any of the preceding claims wherein said counting means is a decade counter.

46. A pulse generating means for generating an output pulse in response to a prescribed sequence of input signals, said sequence corresponding to the receipt of one or more input signals within a fixed time period, comprising

a delay means and a sampling means wherein said delay means outputs an activating signal to said sampling means after a time delay from the receipt of an input signal, and said sampling means generates said output pulse only in response to the presence of an input signal and said activating signal, said time delay approximating said fixed time period.

47. A pulse generating means as claimed at claim 46, wherein said delay means comprises a monostable multivibrator, triggerable in response to a received input signal, and a charging means including a capacitor, said charging means being actuated by the triggering of said monostable, whereby the monostable charges said capacitor to at least a threshold voltage, said threshold voltage causing the monostable to reset, and the charging means generating said activating signal at a time near to or in conjunction with the capacitor attaining said threshold voltage.

48. A pulse generating means as claimed at claim 47 wherein said charging means includes an integrating circuit which integrates the non-inverted output of said monostable to effect generation of said activating signal.

49. A pulse generating means as claimed at claim 48 wherein said charging means includes a voltage divider in series with said capacitor whereby said activating signal is generated at the output of the voltage divider.

50. A pulse generating means as claimed at claim 47 wherein said charging means includes a differentiating circuit which differentiates the inverted output of said monostable to effect generation of said activating signal.

51. A pulse generating means as claimed at any of claims 46 to 50, wherein said sampling means comprises a logic gate having one input corresponding to said input signal and another input corresponding to said activating signal, whereby said output pulse is generated in response to the concurrent presence of an input signal and activating signal.

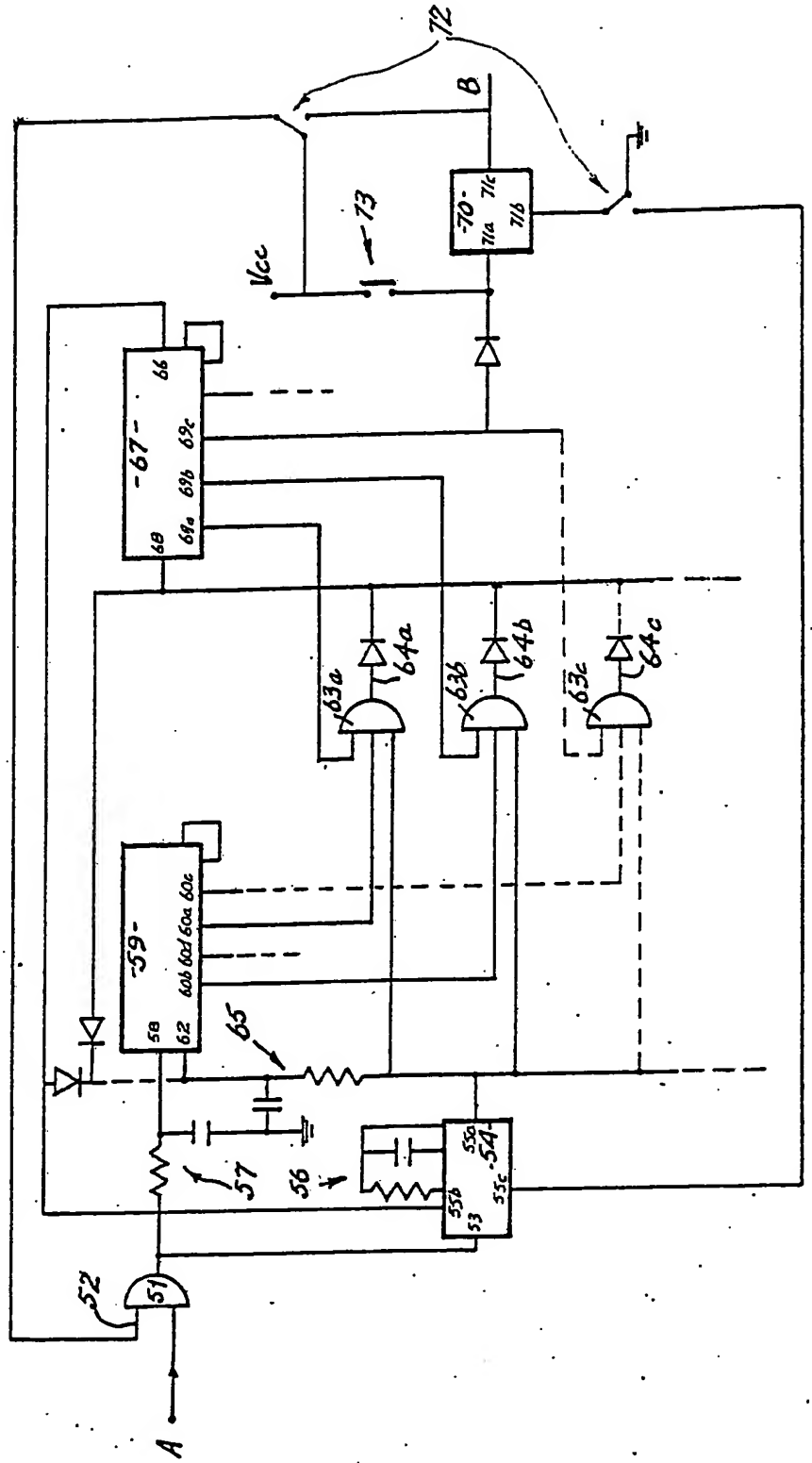

FIG. 2

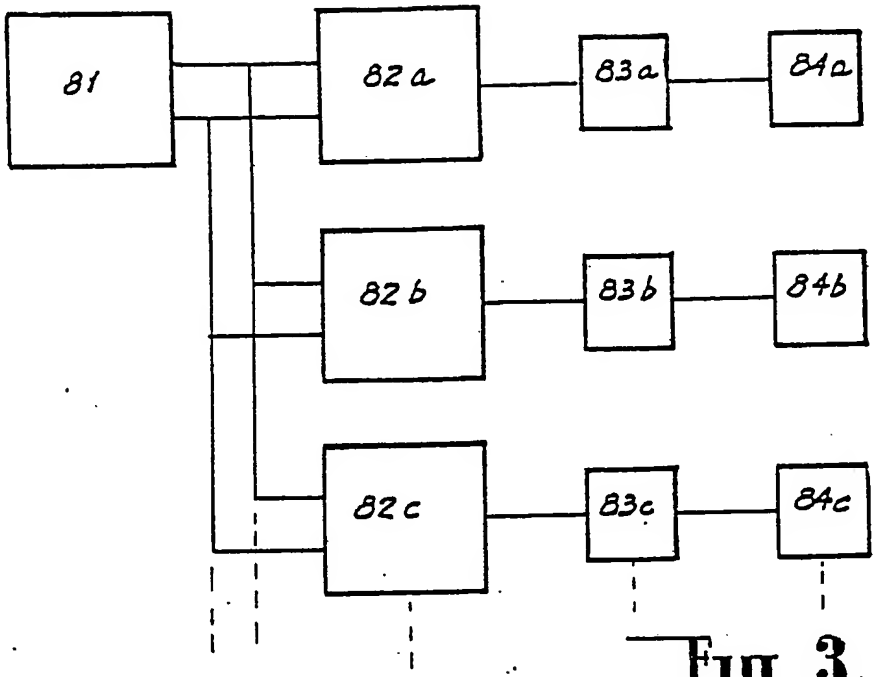

Fig. 3.

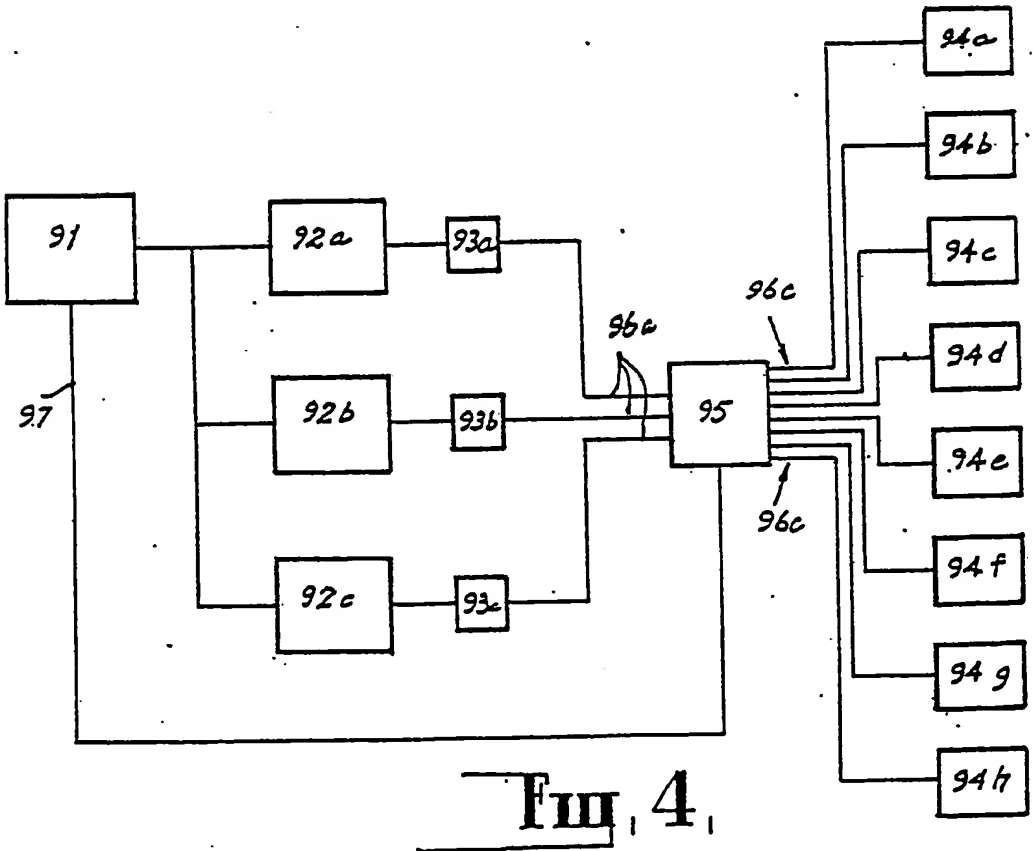

Fig. 4.

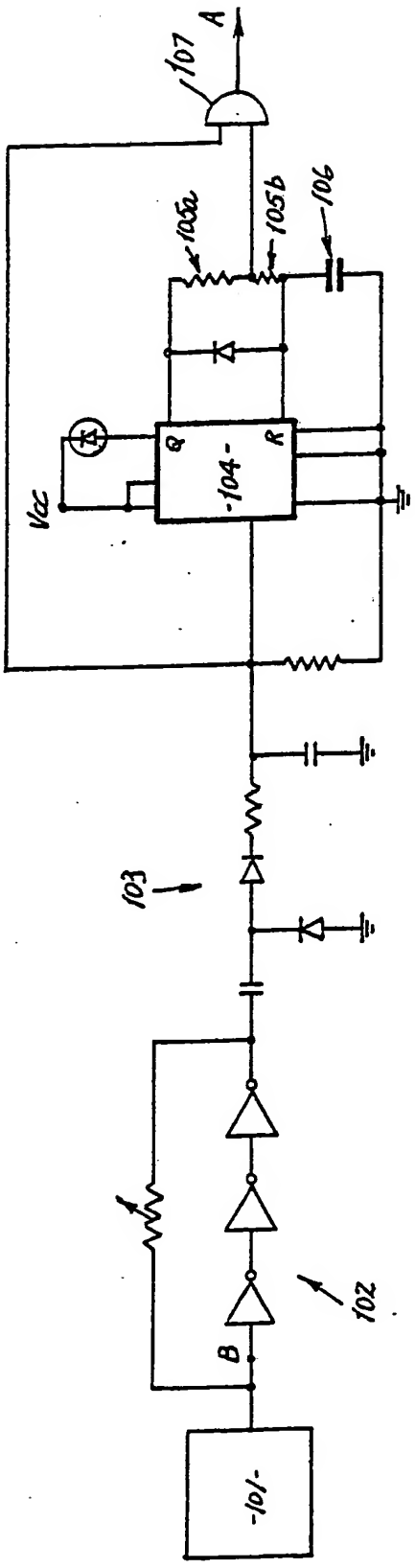

Fig. 5

INTERNATIONAL SEARCH REPORT

International Application No PCT/AU 84/00007

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int. Cl.[3] G08B 1/08, 3/10

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
IPC	G08B 1/08, 3/10, H03K 5/15, 17/14
US	307/518, 340/825.38

Documentation Searched other than Minimum Documentation to the Extent that such Documents are included in the Fields Searched [5]

AU: IPC as above; Australian Classification 99,6, 99.8

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
Y	US, A, 4 146 754 (ROSS) 27 March 1979 (27.03.79)	1, 46
Y	US, A, 4 006 316 (BOLGIANO) 1 February 1977 (01.02.77)	1, 46
A	US, A, 3 876 836 (LANGAN) 8 April 1975 (08.04.75)	1, 46
A	GB, A, 2 103 854 (LGM ELECTRONIC S LTD) 23 February 1983 (23.02.83)	1
A	US, A, 4 313 107 (MORI) 26 January 1982 (26.01.82)	1, 46
A	US, A, 3 384 873 (SHARMA) 21 May 1968 (21.05.68)	1
A	US, A, 3 634 826 (BIEDERMANN) 25 February 1972 (25.02.72)	1
X,E	AU, A, 16912/83 (KENNY) 19 January 1984 (19.01.84)	1, 46

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
27 March 1984 (27.03.84)	3 April 1984 (03.04.84)
International Searching Authority [1]	**Signature of Authorized Officer [20]**
Australian Patent Office	A.S. Moore A.S. Moore

Form PCT/ISA/210 (second sheet) (October 1981)

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/AU 84/00007

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report	Patent Family Members		
US 4006316	US 3936617	US 4001708	US 4081130
US 4313107	AU 42575/78 GB 2011689	CA 1125870	DE 2855301

END OF ANNEX